Enterprise Line Applications

- Vcore power regulation for Intel® VR13 rev1.1 and VR12.5 Rev1.5 based Microprocessors
  - Servers, Workstations, and High-end desktops

Enterprise Line Features

- Compliant to Intel® VR13 and VR12.5 DC-DC converter specifications
- Compliant to Intel® SVID protocol rev1.7
- Output voltage regulation range
  - 0.5V to 2.5V (10mV/step)
  - 0.25V to 1.52V (5mV/step)
- Programmable to support one, two, or three fully digitally controlled voltage rails
- PMBus™ rev 1.2 compliant serial interface
  - Query voltage, current, temperature faults
  - Fault Response
- Supports start-up into pre-bias voltage
- Configurable autonomous phase add/drop
- Digitally programmable PID loop compensation
- Digitally programmable loadline slope and offset
- Digital temperature compensation
- Input (+12V) power estimation
- Extensive fault detection and protection capability
  - IUVP, IOVP, OUVP, OOVP (fixed and tracking)
  - OCP instantaneous, averaged (total current), channel, and pulse-to-pulse current limit protection
  - Multiple internal and external OTP thresholds
  - Open/short voltage sense line detection
  - Negative current limit protection
- Internal non-volatile memory (NVM) for custom configurations
- Combined state-machine and µ-controller core architecture for maximum flexibility
- RoHS compliant and Halogen free QFN plastic package

Enterprise Line Description

The Infineon Technologies enterprise digital controllers provide power for Intel® VR13 and VR12.5 applications. Command and monitor functions are controlled through the SVID interface which supports 5mV/step and 10mV/step VID tables, dynamic voltage identification (DVID), power states (PS), and VR Data & Configuration Register requirements.

Advanced control loop features, such as Active Transient Response (ATR) modulation and fast DVID response enable optimal response to high di/dt load transients and large voltage steps.

Programmable temperature compensation to current sense allows the designer to tailor the response for best loadline accuracy over temperature. Best in class noise immunity is achieved through high oversample rate and digital current estimation. Along with inductor DCR current sensing, enterprise controllers also support Infineon integrated power stages with integrated current sense and integrated temperature sense. Enterprise controllers support either ΔVBE or PTAT temperature sensors which provide accurate loadline performance.

Protection features include a comprehensive suite of sophisticated over-voltage, under-voltage, over-temperature, and over-current protections. Enterprise controllers also detect and protect against an open or short circuit on the remote sensing inputs. These attributes provide a complete and advanced protection feature set for microprocessor and power systems.

Table 1: Enterprise Controller Offerings

Part Number	Configuration	Temp Range	Package	Page
PXE1610CDN	6+1 phase	-5°C to +85°C	48-lead 6mm x 6mm QFN, PG-VQFN-48	4
PXE1110CDM	1+1 phase	-5°C to +85°C	40-lead 5mm x 5mm QFN PG-VQFN-40	7

Memory Line Applications

- DDR3/DDR4 Memory power regulation for Intel® VR13 rev1.1, VR12.5 Rev 1.5 and IMVP8 rev1.2 based systems

Memory Line Features

- Compliant to Intel® DC-DC converter specifications for memory applications
- Compliant to Intel® SVID protocol rev1.7
- Output voltage regulation range
  - 0.5V to 2.5V (10mV/step)
  - 0.25V to 1.52V (5mV/step)
- Programmable to support one, two, or three fully digitally controlled voltage rails
- PMBus™ rev 1.2 compliant serial interface
  - Query voltage, current, temperature faults
  - Fault Response
- Supports start-up into pre-bias voltage
- Configurable autonomous phase add/drop
- Digitally programmable PID loop compensation
- Digital temperature compensation
- Input (+12V) power estimation
- Extensive fault detection and protection capability
  - IUVP, IOVP, OUVP, OOVP (fixed and tracking)
  - OCP instantaneous, averaged (total current), channel, and pulse-to-pulse current limit protection
  - Multiple internal and external OTP thresholds
  - Open/short voltage sense line detection
  - Negative current limit protection
- Internal non-volatile memory (NVM) for custom configurations
- Combined state-machine and µ-controller core architecture for maximum flexibility
- RoHS compliant and Halogen free QFN plastic package

Memory Line Description

The Infineon Technologies memory digital controllers provide intelligent power for today's DDR3/DDR4 applications. Command and monitor functions are controlled through the Intel SVID interface which supports 5mV/step VID table, dynamic voltage identification (DVID), power states (PS), and VR Data & Configuration Register requirements.

Infineon's memory controllers utilize digital technology to implement all control functions, providing the ultimate system solution in terms of flexibility and stability. Advanced control loop features, such as Active Transient Response (ATR) modulation and fast DVID response enable optimal response to high di/dt load transients.

Programmable temperature compensation to current sense allows the designer to tailor the response for best loadline accuracy over temperature. Best in class noise immunity is achieved through high oversample rate and digital current estimation. Along with inductor DCR current sensing, memory controllers also support Infineon power stages with integrated current sense and integrated temperature sense. Memory controllers support either ΔVBE or PTAT temperature sensors which provide accurate loadline performance.

Protection features include a comprehensive suite of sophisticated over-voltage, under-voltage, over-temperature, and over-current protections. Memory controllers also detect and protect against an open or short circuit on the remote sensing inputs. These attributes provide a complete and advanced protection feature set for microprocessor and power systems.

Table 2: Memory Controller Offerings

Part Number	Configuration	Temp Range	Package	Page
PXM1310CDM	3+1 phase	-5°C to +85°C	40-lead 5mm x 5mm QFN PG-VQFN-40	10

Absolute Maximum Ratings

Subjecting the controller to stresses above those listed in Table 3 may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure to the absolute maximum ratings for extended periods may adversely affect the operation and reliability of the device.

Table 3: Absolute Maximum Ratings

Symbol	Description	Min	Max	Units	Conditions
VDD	Supply voltage	-0.3	4	V	Note A
VCLK, VDIO, VALRT#		-0.3	1.35	V	
AVSEN, BVSEN, CVSEN		-0.3	3.7	V	Do not exceed VDD + 0.2V
AVREF, BVREF, CVREF		-0.3	0.5	V	
ISENx, IREFx	DCR current sense	-0.3	3.7	V	Do not exceed VDD + 0.2V
	Integrated current sense	-0.3	2.0	V	
VD12		-1	1	mA	Do not drive or load this pin
	All other pins	-0.30	4*	V	Note A, Note B
T_J	Junction temperature	-40	125	°C	
T_{STG}	Storage temperature	-65	150	°C	
T_{LEAD}	Lead temperature		300	°C	Soldering, 10 seconds

Note A: The absolute maximum VDD supply voltage is 4.0V with the conditions that the junction temperature range is maintained between -40℃ ≤ T_J ≤ +125℃ and the product is not operated at the absolute maximum VDD supply voltage for more than 24 hours cumulatively over the lifetime of the product.

*Note B: *The lesser of 4V or VDD+0.2V; outputs in Hi-Z state*

Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Symbol	Description	Min	Nom	Max	Units	Notes
VDD	Supply voltage	+3.0	+3.3	+3.6	V	
T_A	Ambient temperature range	-5	25	85	°C	Applicable to “PX…CDM” and “PX…CDN” devices only
T_J	Junction temperature	-40	25	125	°C	Applicable to “PX…CPM” and “PX…CPN” devices only

Table 5: Temperature Information

Symbol	Description	6mm x 6mm QFN	5mm x 5mm QFN
$\theta_{JA(0)}$	Junction-to-ambient thermal resistance at 0 lfm	30.3°C/W	28.4°C/W
$\theta_{JA(200)}$	Junction-to-ambient thermal resistance at 200 lfm	26.2°C/W	25.1°C/W
$\theta_{JA(500)}$	Junction-to-ambient thermal resistance at 500 lfm	23.4°C/W	22.8°C/W
θ_{JC}	Junction-to-case thermal resistance	2.8°C/W	2.8°C/W

PXE1610 General Description

The PXE1610 digital dual rail 6+1 phase controller provides power for Intel® VR13 server applications. Core voltage is provided by a multi-phase buck converter with up to six synchronous-rectified channels in parallel while a single phase second rail provides voltage for the I/O.

Package Pin Designations

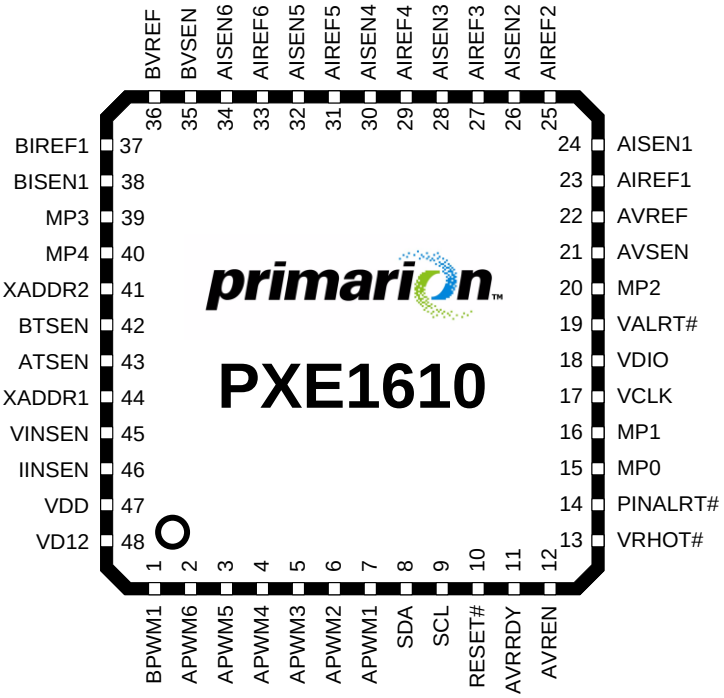


Table 6: PXE1610 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	BPWM1	O	3.3V CMOS	Loop_B phase #1 PWM output. Refer to APWM1 description.
2	APWM6	O	3.3V CMOS	Loop_A phase #6 PWM output. Refer to APWM1 description.
3	APWM5	O	3.3V CMOS	Loop_A phase #5 PWM output. Refer to APWM1 description.
4	APWM4	O	3.3V CMOS	Loop_A phase #4 PWM output. Refer to APWM1 description.
5	APWM3	O	3.3V CMOS	Loop_A phase #3 PWM output. Refer to APWM1 description.
6	APWM2	O	3.3V CMOS	Loop_A phase #2 PWM output. Refer to APWM1 description.
7	APWM1	O	3.3V CMOS	Loop_A phase #1 Pulse Width Modulation (PWM) output. This signal is used to drive the PWM input of the power stage/FET driver IC. Unused PWM pins should be left unconnected (floating).
8	SDA	I/O	Open Drain	SMBus/I2C bi-directional serial data signal
9	SCL	I/O	Open Drain	SMBus/I2C bi-directional serial clock signal
10	RESET#	I	3.3V CMOS	RESET# feature allows controller to be put into lowest power dissipation mode. This pin may be left floating if unused but it is recommended that a 1kΩ pull up to 3.3V be used if this signal is connected to a trace on the board.

Pin #	Name	I/O	Type	Description
11	AVRRDY	O	Open Drain	Voltage regulator “Ready” output signal. The AVRRDY indicator will be asserted when the controller is ready to accept SVID commands after AVREN is asserted. This open-drain output requires an external pull-up resistor (1k · recommended). AVRRDY will be pulled low when a shutdown fault occurs.
12	AVREN	I	1.2V CMOS Note G	Active high Output Enable input. Asserting the AVREN pin will activate the digital controller, pending status of the internal power-on-reset circuit and any existing fault states. De-asserting then asserting AVREN after a latched-fault based shutdown will cause the controller to enter the soft-start state. Faults will be cleared when AVREN is reasserted.
13	VRHOT#	O	Open Drain	Active low external temperature indicator. VRHOT# is asserted at the temperature defined by the programmable TEMP_MAX register.
14	PINALRT#	O	Open Drain	Active low external input supply power alert. PINALRT# is asserted when the input power reaches the threshold defined by the programmable PIN_MAX register. Unused PINALRT# may be left open.
15	MP0	I/O	Note D	Multi-purpose pin-0 configurable as BVRRDY, FAULT1, FAULT2, ADREN, BDREN, or LPM; Unused MP pins may be left open. Note C. Note F
16	MP1	I/O	Note D	Multi-purpose pin-1 configurable as BVREN, BVRRDY, FAULT1, FAULT2, ADREN, BDREN, or SMBAlert#; Note C. Note F
17	VCLK	I	1.2V CMOS	SVID clock interface. Note E
18	VDIO	I/O	Open Drain	SVID bi-directional data interface. Note E
19	VALRT#	O	Open Drain	SVID active low ALERT# signal. This output is asserted to indicate the status of the VR has changed. Note E
20	MP2	I/O	Note D	Multi-purpose pin-2 configurable as FAULT2, SMBAlert#, or IMON. Note F
21	AVSEN	I	Analog	Loop_A voltage sense inputs. AVSEN (+) and AVREF (-) are inputs to the precision differential remote sense amplifier and should be connected to the sense pins of the remote load. To attenuate high frequency noise coupled onto the sense lines, it is recommended that an RC filter (10Ω and 220pF) be placed close to the controller.
22	AVREF	I	Analog	
23	AIREF1	I	Analog	Loop_A phase #1 current sense inputs. The AIREF1 (-) and AISEN1 (+) pins are used to differentially sense the corresponding channel current. The sensed current is used for channel-to-channel current balancing, loadline regulation, and over-current protection. Unused AIREFx/AISENx pins may be left open or tied to ground.
24	AISEN1	I	Analog	
25	AIREF2	I	Analog	Loop_A phase #2 current sense inputs. Refer to AIREF1/AISEN1 description.
26	AISEN2	I	Analog	
27	AIREF3	I	Analog	Loop_A phase #3 current sense inputs. Refer to AIREF1/AISEN1 description
28	AISEN3	I	Analog	
29	AIREF4	I	Analog	Loop_A phase #4 current sense inputs. Refer to AIREF1/AISEN1 description
30	AISEN4	I	Analog	
31	AIREF5	I	Analog	Loop_A phase #5 current sense inputs. Refer to AIREF1/AISEN1 description
32	AISEN5	I	Analog	
33	AIREF6	I	Analog	Loop_A phase #6 current sense inputs. Refer to AIREF1/AISEN1 description
34	AISEN6	I	Analog	

Pin #	Name	I/O	Type	Description
35	BVSEN	I	Analog	Loop_B voltage sense inputs. Refer to AVSEN/AVREF description. If unused, these pins may be grounded or left open.
36	BVREF	I	Analog	
37	BIREF1	I	Analog	Loop_B current sense inputs. Refer to AIREF1/AISEN1 description. If Loop_B is not used, these pins may be left open/grounded.
38	BISEN1	I	Analog	
39	MP3	I/O	Note D	Multi-purpose pin-3 configurable as FAULT2 or SMBAlert#; Note C. Note F
40	MP4	I/O	Note D	Multi-purpose pin-4 configurable as FAULT2 or SMBAlert#; Note C. Note F
41	XADDR2	I	Analog	Used in conjunction with XADDR1, the I2C address of the controller is set by tying an external resistor between this pin and GND.
42	BTSEN	I	Analog	Loop_B external temperature sense input. Refer to ATSEN description.
43	ATSEN	I	Analog	Loop_A external temperature sense input. If the digital controllers' internal temperature sensor is selected and/or the external temperature reporting is not required, the ATSEN pin may be left open (floating).
44	XADDR1	I	Analog	Used in conjunction with XADDR2, the I2C address of the controller is set by tying an external resistor between this pin and GND.
45	VINSEN	I	Analog	VIN (+12V) voltage sense input. The VINSEN pin may be connected to the +12V supply through a resistor divider, or to the PI sense network and is used to guarantee a valid input voltage before starting up (input under-voltage lockout). Refer to the *Power Input Sense* section herein for details. If unused, this pin may be grounded.
46	IINSEN	I	Analog	Current sense input used for PWR_IN calculation. An external amplifier or the PI sense network may be used to translate current information from a precision sense resistor to an input signal for the controller. Refer to the *Power Input Sense* section herein for details. If unused, this pin may be grounded.
47	VDD	S	supply	3.3V power supply input to the digital controller. This pin should be connected to the system +3.3V supply and decoupled using high quality 1.0µF + 0.1µF ceramic capacitors.
48	VD12	S	Internal Supply	Do not apply voltage to or ground this pin. Internally generated 1.2V voltage reference used to power digital core logic. The pin is provided for attaching external decoupling capacitors only. Decouple using high quality 1.0µF + 0.1µF ceramic capacitors. This pin is not intended to be used to drive external components as +1.2V reference.
Die Paddle		S	Ground	Exposed Ground pad beneath the device must be soldered to the PCB ground for proper operation.

Note C: ADREN/BDREN/CDREN = Loop_A/B/C Driver Enable. BVRRDY/CVRRDY = Loop_B/C VR Ready. BVREN/CVREN = Loop_B/C VR Enable. LPM = Low Power Mode. PXE1xxxC is pin-to-pin compatible with PXE1xxxB with equivalent, improved, or expanded capability.

Note D: Programmable: depending on the selected function, the MPx pin may be programmed to 3.3V CMOS, Open Drain, or Analog.

Note E: If the SVID interface is not used, the pins need to be tied together and pulled-up to VD12 through a 1K resistor.

Note F: During device power up, this pin will be internally shorted to GND for a maximum of 21 ms. If the pin is configured for use as a digital input to the controller, it is recommended a 200Ω current limiting resistor be connected in series between the pin and the signal source.

Note G: There is no internal biasing on AVREN. This pin must not be left open.

PXE1110 General Description

The PXE1110 digital dual rail 1+1 phase controller provides power for Intel® VR13 server applications. Users have the option to order PXE1110 parts with either parallel-VID or SVID control. For parallel-VID parts, only one loop can be set to follow the parallel-VID setting. The other loop will stay at Vboot. Users may set the VID of both loops through I2C commands. Contact Infineon FAE for details.

Package Pin Designations

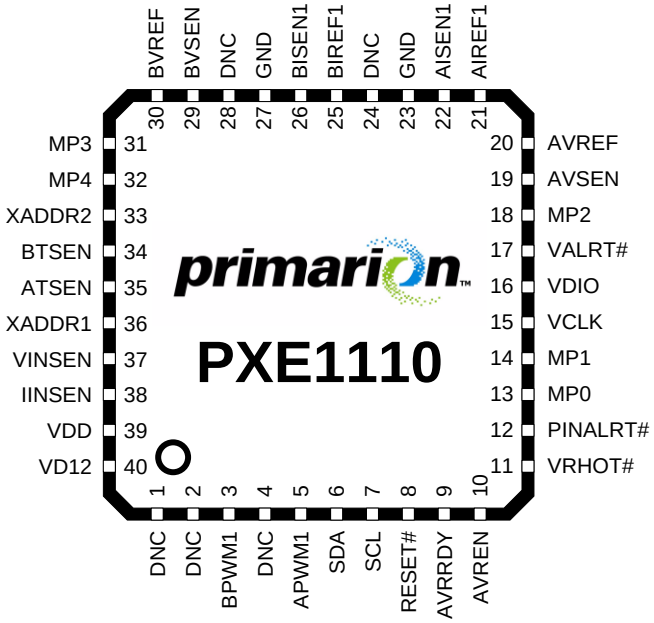


Table 7: PXE1110 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	DNC			Do not connect (leave floating).
2	DNC			Do not connect (leave floating).
3	BPWM1	O	3.3V CMOS	Loop_B phase #1 PWM output. Refer to APWM1 description.
4	DNC			Do not connect (leave floating).
5	APWM1	O	3.3V CMOS	Loop_A phase #1 Pulse Width Modulation (PWM) output. This signal is used to drive the PWM input of the power stage/FET driver IC. Unused PWM pins should be left unconnected (floating).
6	SDA	I/O	Open Drain	SMBus/I2C bi-directional serial data signal.
7	SCL	I/O	Open Drain	SMBus/I2C bi-directional serial clock signal.
8	RESET#	I	3.3V CMOS	RESET# feature allows controller to be put into lowest power dissipation mode. This pin may be left floating if unused but it is recommended that a 1kΩ pull up to 3.3V be used if this signal is connected to a trace on the board.
9	AVRRDY	O	Open Drain	Voltage regulator “Ready” output signal. The AVRRDY indicator will be asserted when the controller is ready to accept SVID commands after AVREN is asserted. This open-drain output requires an external pull-up resistor (1kΩ recommended). AVRRDY will be pulled low when a shutdown fault occurs.

Pin #	Name	I/O	Type	Description
10	AVREN	I	1.2V CMOS Note G	Active high Output Enable input. Asserting the AVREN pin will activate the digital controller, pending status of the internal power-on-reset circuit and any existing fault states. De-asserting then asserting AVREN after a latched-fault based shutdown will cause the controller to enter the soft-start state. Faults will be cleared when AVREN is reasserted.
11	VRHOT#	O	Open Drain	Active low external temperature indicator. VRHOT# is asserted at the temperature defined by the programmable TEMP_MAX register.
12	PINALRT#	O	Open Drain	Active low external input supply power alert. PINALRT# is asserted when the input power reaches the threshold defined by the programmable PIN_MAX register. Unused PINALRT# may be left open.
13	MP0	I/O	Note D	Multi-purpose pin-0 configurable as BVRRDY, FAULT1, FAULT2, ADREN, BDREN, or LPM. Unused MP pins may be left open. Note F
14	MP1	I/O	Note D	Multi-purpose pin-1 configurable as BVREN, BVRRDY, FAULT1, FAULT2, ADREN, BDREN, or SMBAlert#. Note F
15	VCLK	I	1.2V CMOS	SVID clock interface. Note E
16	VDIO	I/O	Open Drain	SVID bi-directional data interface. Note E
17	VALRT#	O	Open Drain	SVID active low ALERT# signal. This output is asserted to indicate the status of the VR has changed. Note E
18	MP2	I/O	Note D	Multi-purpose pin-2 configurable as FAULT2, SMBAlert#, or IMON. Note F
19	AVSEN	I	Analog	Loop_A voltage sense inputs. AVSEN (+) and AVREF (-) are inputs to the precision differential remote sense amplifier and should be connected to the sense pins of the remote load. To attenuate high frequency noise coupled onto the sense lines, it is recommended that an RC filter (10Ω and 220pF) be placed close to the controller.
20	AVREF	I	Analog	
21	AIREF1	I	Analog	Loop_A phase #1 current sense inputs. The AIREF1 (-) and AISEN1 (+) pins are used to differentially sense the corresponding channel current. The sensed current is used for channel-to-channel current balancing, loadline regulation, and over-current protection. Unused AIREFx/AISENx pins may be left open or tied to ground.
22	AISEN1	I	Analog	
23	GND			Tie pin directly to GND (no internal connection to GND).
24	DNC			Do not connect (leave floating).
25	BIREF1	I	Analog	Loop_B current sense inputs. Refer to AIREF1/AISEN1 description. If Loop_B is not used, these pins may be left open/grounded.
26	BISEN1	I	Analog	
27	GND			Tie pin directly to GND (no internal connection to GND).
28	DNC			Do not connect (leave floating).
29	BVSEN	I	Analog	Loop_B voltage sense inputs. Refer to AVSEN/AVREF description.
30	BVREF	I	Analog	
31	MP3	I/O	Note D	Multi-purpose pin-3 configurable as FAULT2 or SMBAlert#. Note F
32	MP4	I/O	Note D	Multi-purpose pin-4 configurable as FAULT1 or SMBAlert#. Note F
33	XADDR2	I	Analog	Used in conjunction with XADDR1, the I2C address of the controller is set by tying an external resistor between this pin and GND.
34	BTSEN	I	Analog	Loop_B external temperature sense input. Refer to ATSEN description.

Pin #	Name	I/O	Type	Description
35	ATSEN	I	Analog	Loop_A external temperature sense input. If the digital controllers' internal temperature sensor is selected and/or the external temperature reporting is not required, the ATSEN pin may be left open (floating).
36	XADDR1	I	Analog	Used in conjunction with XADDR2, the I2C address of the controller is set by tying an external resistor between this pin and GND.
37	VINSEN	I	Analog	VIN (+12V) voltage sense input. The VINSEN pin may be connected to the +12V supply through a resistor divider, or to the PI sense network and is used to guarantee a valid input voltage before starting up (input under-voltage lockout). Refer to the *Power Input Sense* section herein for details. If unused, this pin may be grounded.
38	IINSEN	I	Analog	Current sense input used for PWR_IN calculation. An external amplifier or the PI sense network may be used to translate current information from a precision sense resistor to an input signal for the controller. Refer to the *Power Input Sense* section herein for details. If unused, this pin may be grounded.
39	VDD	S	supply	3.3V power supply input to the digital controller. This pin should be connected to the system +3.3V supply and decoupled using high quality 1.0µF + 0.1µF ceramic capacitors.
40	VD12	S	Internal Supply	Do not apply voltage to or ground this pin. Internally generated 1.2V voltage reference used to power digital core logic. The pin is provided for attaching external decoupling capacitors only. Decouple using high quality 1.0µF + 0.1µF ceramic capacitors. This pin is not intended to be used to drive external components as +1.2V reference.
Die Paddle		S	Ground	Exposed Ground pad beneath the device must be soldered to the PCB ground for proper operation.

PXM1310 General Description

The PXM1310 digital dual rail 3+1 phase controller provides power for Intel® VR13 memory applications. One output voltage is provided by a 3-phase buck converter operating with up to three synchronous-rectified channels in parallel while a single-phase buck converter provides voltage for the VPP rail.

Package Pin Designations

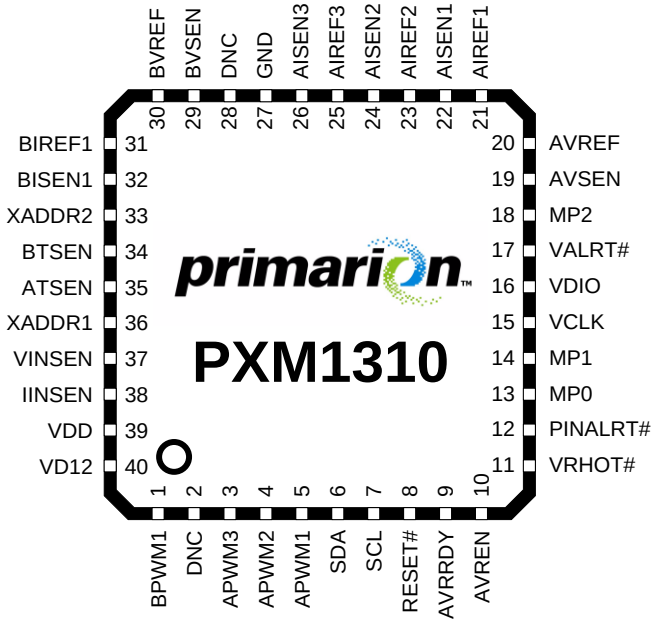


Table 8: PXM1310 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	BPWM1	O	3.3V CMOS	Loop_B PWM output. Refer to APWM1 description.
2	DNC			Do not connect (leave floating).
3	APWM3	O	3.3V CMOS	Loop_A phase #3 PWM output. Refer to APWM1 description.
4	APWM2	O	3.3V CMOS	Loop_A phase #2 PWM output. Refer to APWM1 description.
5	APWM1	O	3.3V CMOS	Loop_A phase #1 Pulse Width Modulation (PWM) output. This signal is used to drive the PWM input of the power stage/FET driver IC. Unused PWM pins should be left unconnected (floating).
6	SDA	I/O	Open Drain	SMBus/I2C bi-directional serial data signal.
7	SCL	I/O	Open Drain	SMBus/I2C bi-directional serial clock signal.
8	RESET#	I	3.3V CMOS	RESET# feature allows controller to be put into lowest power dissipation mode. This pin may be left floating if unused but it is recommended that a 1kΩ pull up to 3.3V be used if this signal is connected to a trace on the board.
9	AVRRDY	O	Open Drain	Voltage regulator “Ready” output signal. The AVRRDY indicator will be asserted when the controller is ready to accept SVID commands after AVREN is asserted. This open-drain output requires an external pull-up resistor (1kΩ recommended). AVRRDY will be pulled low when a shutdown fault occurs.

Pin #	Name	I/O	Type	Description
10	AVREN	I	1.2V CMOS	Active high Output Enable input. Asserting the AVREN pin will activate the digital controller, pending status of the internal power-on-reset circuit and any existing fault states. De-asserting then asserting AVREN after a latched-fault based shutdown will cause the controller to enter the soft-start state. Faults will be cleared when AVREN is reasserted.
11	VRHOT#	O	Open Drain	Active low external temperature indicator. VRHOT# is asserted at the temperature defined by the programmable TEMP_MAX register.
12	PINALRT#	O	Open Drain	Active low external input supply power alert. PINALRT# is asserted when the input power reaches the threshold defined by the programmable PIN_MAX register. Unused PINALRT# may be left open.
13	MP0	I/O	Note D	Multi-purpose pin-0 configurable as BVRRDY, FAULT1, FAULT2, ADREN, BDREN, or LPM. Unused MP pins may be left open. Note F
14	MP1	I/O	Note D	Multi-purpose pin-1 configurable as BVREN, BVRRDY, FAULT1, FAULT2, ADREN, BDREN, or SMBAlert#. Note F
15	VCLK	I	1.2V CMOS	SVID clock interface. Note E
16	VDIO	I/O	Open Drain	SVID bi-directional data interface. Note E
17	VALRT#	O	Open Drain	SVID active low ALERT# signal. This output is asserted to indicate the status of the VR has changed. Note E
18	MP2	I/O	Note D	Multi-purpose pin-2 configurable as FAULT2, SMBAlert#, or IMON. Note F
19	AVSEN	I	Analog	Loop_A voltage sense inputs. AVSEN (+) and AVREF (-) are inputs to the precision differential remote sense amplifier and should be connected to the sense pins of the remote load. To attenuate high frequency noise coupled onto the sense lines, it is recommended that an RC filter (10Ω and 220pF) be placed close to the controller.
20	AVREF	I	Analog	
21	AIREF1	I	Analog	Loop_A phase #1 current sense inputs. The AIREF1 (-) and AISEN1 (+) pins are used to differentially sense the corresponding channel current. The sensed current is used for channel-to-channel current balancing, loadline regulation, and over-current protection. Unused AIREFx/AISENx pins may be left open or tied to ground.
22	AISEN1	I	Analog	
23	AIREF2	I	Analog	Loop_A phase #2 current sense inputs. Refer to AIREF1/AISEN1 description.
24	AISEN2	I	Analog	
25	AIREF3	I	Analog	Loop_A phase #3 current sense inputs. Refer to AIREF1/AISEN1 description.
26	AISEN3	I	Analog	
27	GND			Tie pin directly to GND (no internal connection to GND).
28	DNC			Do not connect (leave floating).
29	BVSEN	I	Analog	Loop_B voltage sense inputs. Refer to AVSEN/AVREF description. If unused, these pins should be grounded or left open.
30	BVREF	I	Analog	
31	BIREF1	I	Analog	Loop_B current sense inputs. Refer to AIREF1/AISEN1 description. If Loop_B is not used, these pins may be left open/grounded.
32	BISEN1	I	Analog	
33	XADDR2	I	Analog	Used in conjunction with XADDR1, the I2C address of the controller is set by tying an external resistor between this pin and GND.
34	BTSEN	I	Analog	Loop_B external temperature sense input. Refer to ATSEN description.
35	ATSEN	I	Analog	Loop_A external temperature sense input. If the digital controllers' internal temperature sensor is selected and/or the external temperature reporting is not required, the ATSEN pin may be left open (floating).

Pin #	Name	I/O	Type	Description
36	XADDR1	I	Analog	Used in conjunction with XADDR2, the I2C address of the controller is set by tying an external resistor between this pin and GND.
37	VINSEN	I	Analog	VIN (+12V) voltage sense input. The VINSEN pin may be connected to the +12V supply through a resistor divider, or to the PI sense network and is used to guarantee a valid input voltage before starting up (input under-voltage lockout). Refer to the *Power Input Sense* section herein for details. If unused, this pin may be grounded.
38	IINSEN	I	Analog	Current sense input used for PWR_IN calculation. An external amplifier or the PI sense network may be used to translate current information from a precision sense resistor to an input signal for the controller. Refer to the *Power Input Sense* section herein for details. If unused, this pin may be grounded.
39	VDD	S	supply	3.3V power supply input to the digital controller. This pin should be connected to the system +3.3V supply and decoupled using high quality 1.0µF + 0.1µF ceramic capacitors.
40	VD12	S	Internal Supply	Do not apply voltage to or ground this pin. Internally generated 1.2V voltage reference used to power digital core logic. The pin is provided for attaching external decoupling capacitors only. Decouple using high quality 1.0µF + 0.1µF ceramic capacitors. This pin is not intended to be used to drive external components as +1.2V reference.
Die Paddle		S	Ground	Exposed Ground pad beneath the device must be soldered to the PCB ground for proper operation.

Physical Characteristics – sawn QFN

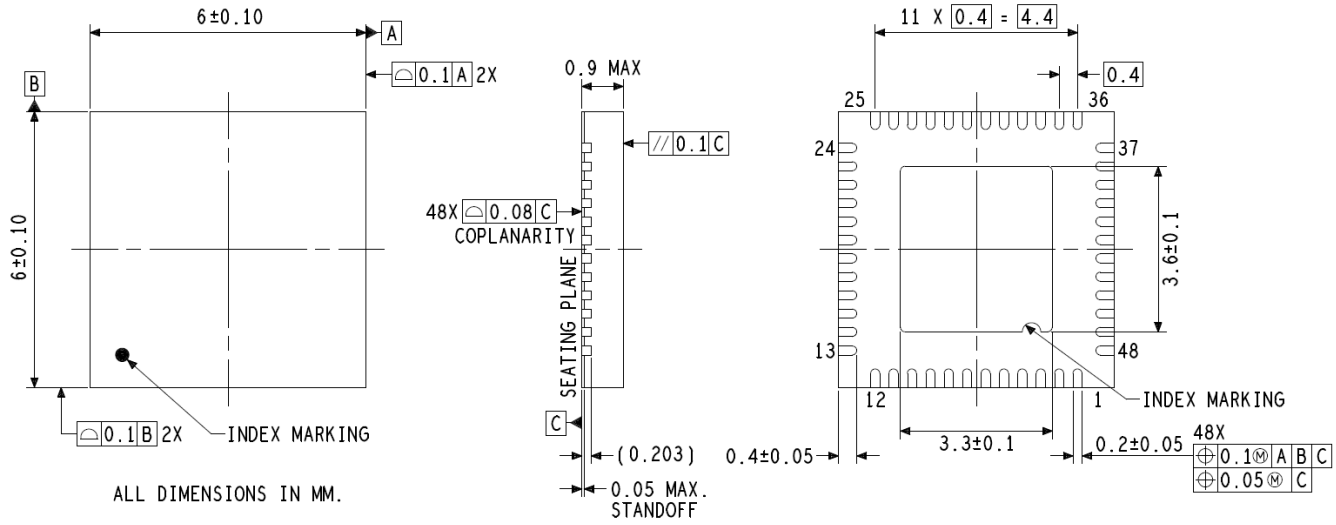


Figure 1. 48-lead sawn QFN, 6mm x 6mm Package Dimensions

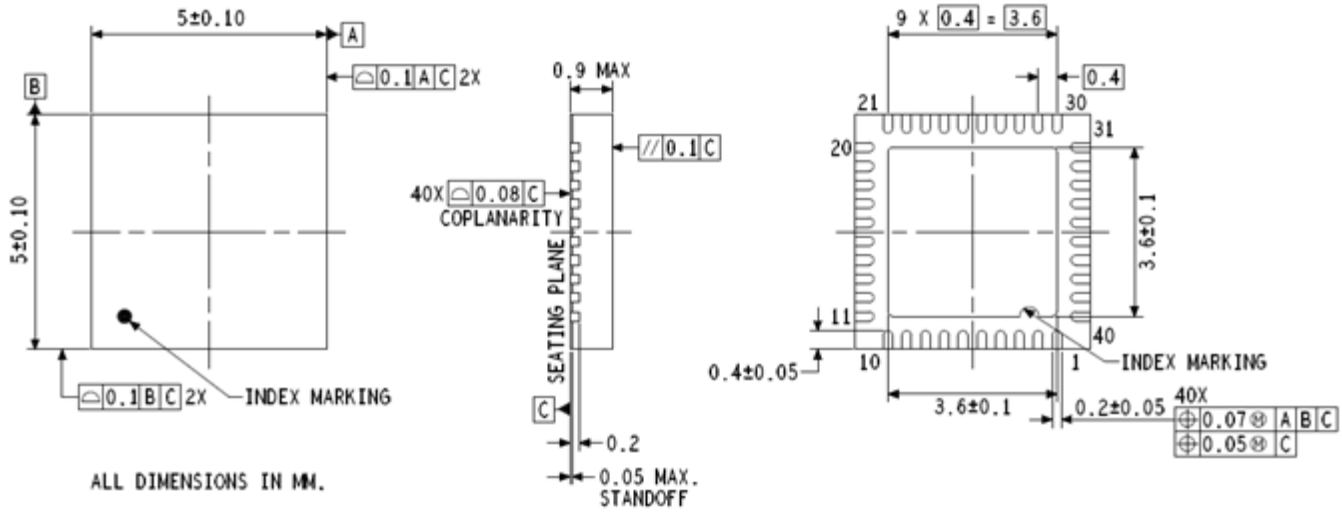


Figure 2. 40-lead sawn QFN, 5mm x 5mm Package Dimensions

Physical Characteristics – punched QFN

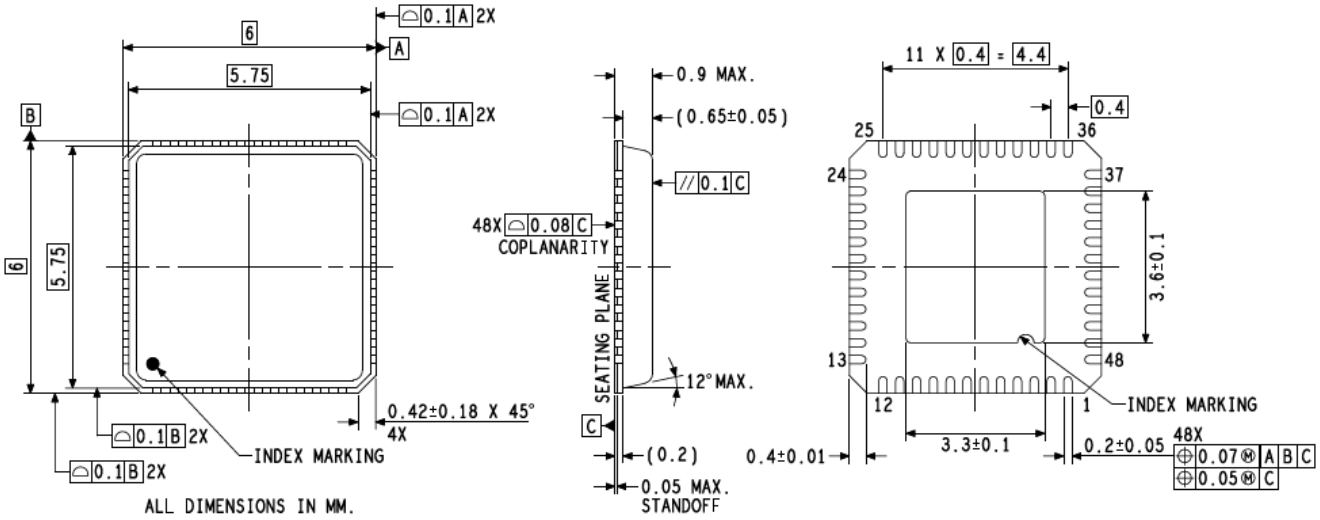


Figure 3. 48-lead punched sawn QFN, 6mm x 6mm Package Dimensions

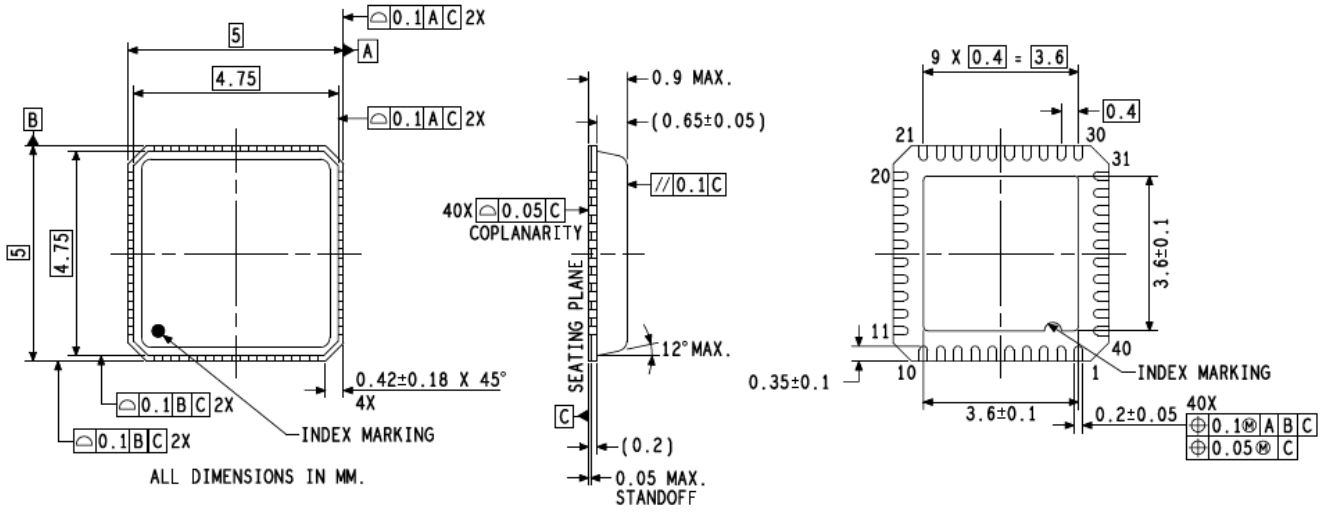
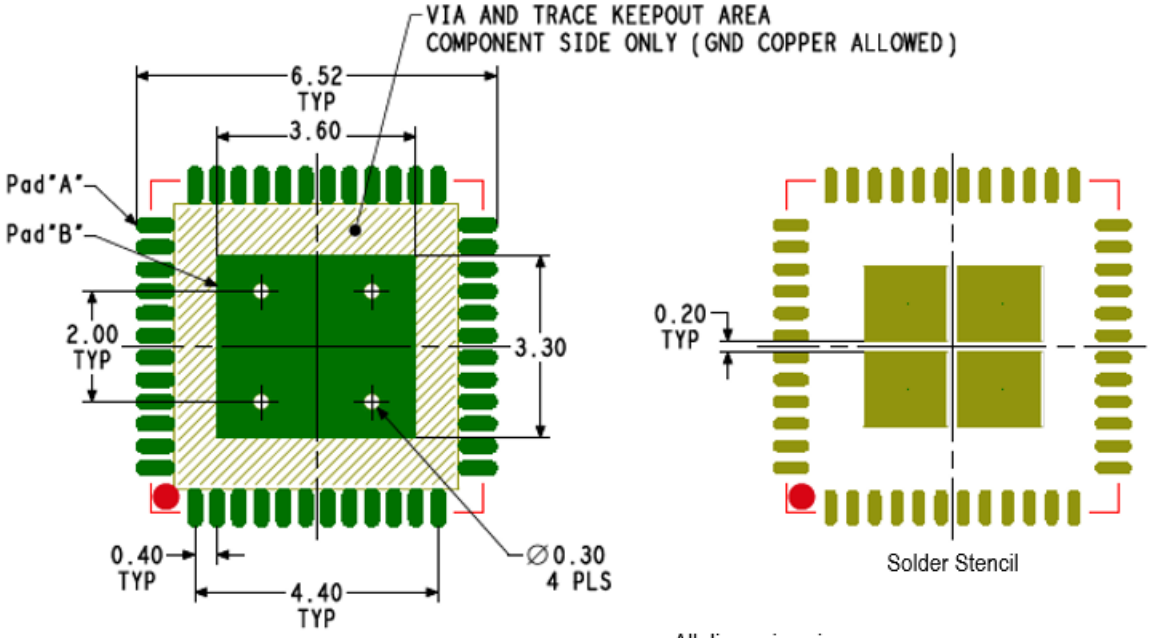


Figure 4. 40-lead punched QFN, 5mm x 5mm Package Dimensions

Package Layout Guidelines

Enterprise and memory controllers are built in either a 48-lead QFN package, or a 40-lead QFN package. Both packages use a solid ring frame and the thermal pad design on the board should be based on the exposed paddle area as shown in Figure 5 and Figure 6 for the 48-lead and 40-lead QFN packages, respectively.

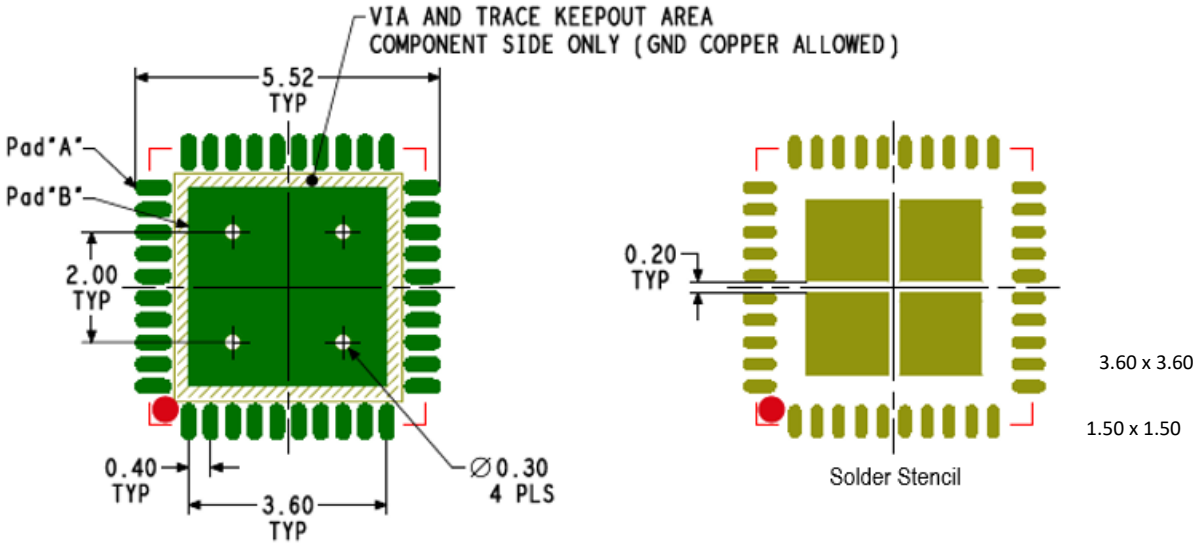
The QFN package is designed to provide superior thermal performance which is mainly achieved by incorporating an exposed die paddle on the bottom surface of the package. However, in order to take full advantage of this feature, the PCB must be designed to effectively conduct heat away from the package. This can be achieved by incorporating a thermal pad along with thermal vias directly under the package. While the thermal pad provides a solderable surface on the top surface of the PCB (to solder the package die paddle onto the board), thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat.



All dimensions in mm

	Pad"A" (48X)	Pad"B"
Pad	0.69 x 0.26	3.60 x 3.30
Solder Mask	0.79 x 0.36	3.70 x 3.40
Solder Paste	0.63 x 0.20	1.50 x 1.35 (4X)

Figure 5: 48-Lead QFN Package Paddle Dimensions (sawn and punched)



All dimensions in mm

	Pad"A" (40X)	Pad"B"
Pad	0.64 x 0.26	3.60 x 3.60
Solder Mask	0.74 x 0.36	3.70 x 3.70
Solder Paste	0.58 x 0.20	1.50 x 1.50 (4X)

Figure 6: 40-Lead QFN Package Paddle Dimensions (sawn and punched)

Ordering Information

Prototype Samples

For preliminary evaluation and engineering builds using Enterprise controllers, it is recommended that customers order samples that have been pre-programmed at the factory with a generic configuration file. The devices with generic file will not regulate by default. The customer can then program the parts to their specific system requirements using software/hardware available from Infineon or through other controller programming facilities (contact Infineon for recommendations). Infineon Field Application Engineers are available to assist with system and configuration file optimization and programming of the controllers. Samples ordered with the generic configuration option will have the shortest lead time. Alternatively, samples can be ordered with a customer specific custom configuration pre-programmed at the factory, but lead times for these types of samples are significantly longer than for generically configured samples. The generic part numbering format is shown below:

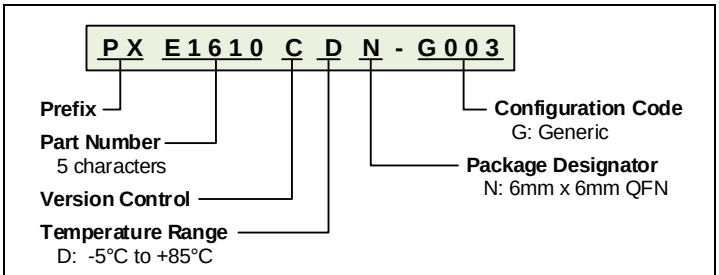


Figure 7. PXE1610CDN Prototype

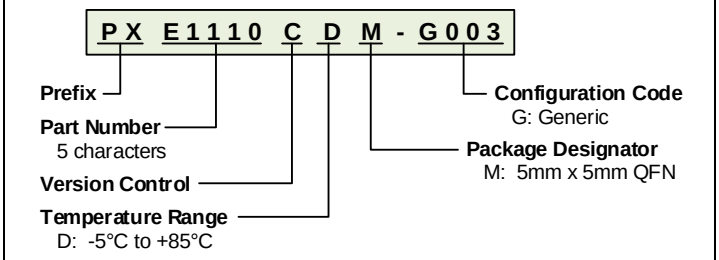


Figure 8. PXE1110CDM Prototype

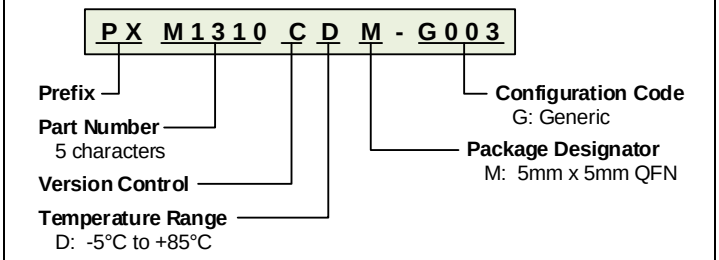


Figure 9. PXM1310CDM Prototype

Production Orders

For high volume/production orders, most customers will want to order Enterprise controllers which have been custom configured at the factory. The part numbering format for custom configured parts is shown below. It is essential that configuration files be reviewed and approved by Infineon prior to ordering large volumes of product:

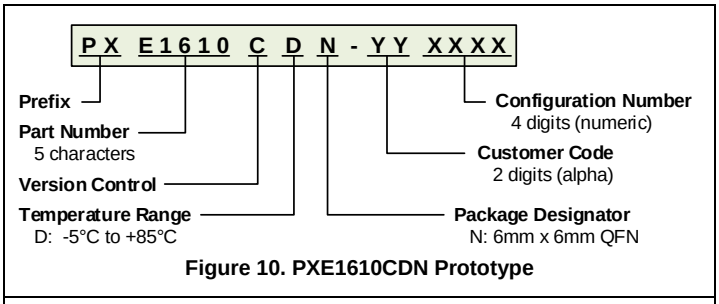


Figure 10. PXE1610CDN Prototype

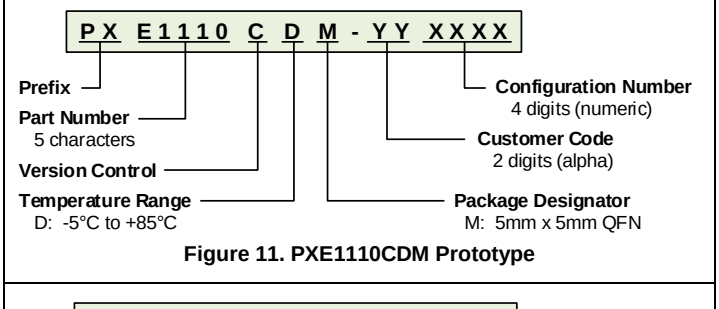


Figure 11. PXE1110CDM Prototype

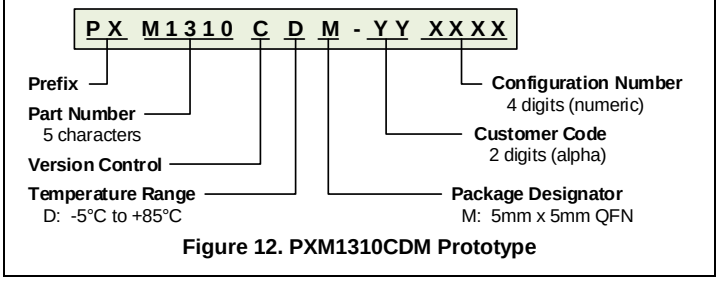


Figure 12. PXM1310CDM Prototype

Part Marking

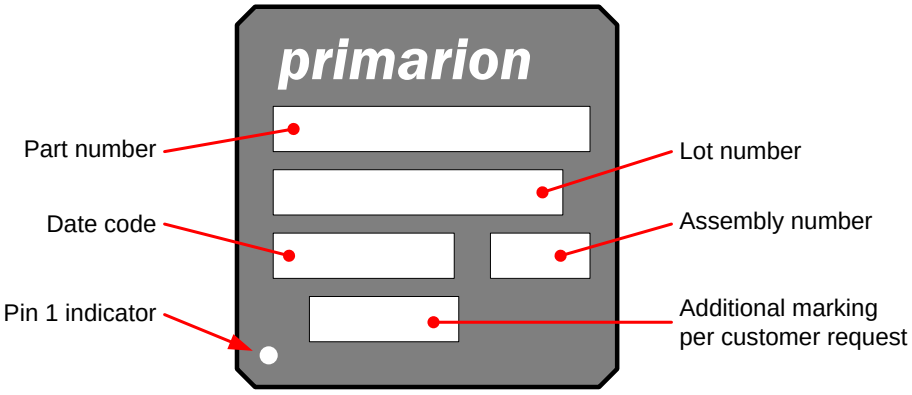


Figure 13. Part Marking

Table 9: Document Revision History

Revision	Description	Date
RevA	• Initial release	June, 2020

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